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IGBT WITH CHANNEL RESISTORS

Background

Insulated gate bipolar transistors (IGBTs) are popular control devices for automobile ignition systems. The IGBT can carry large currents with very low resistance and can be rapidly switched on and off with a low voltage gate. They combine the control characteristics of DMOS devices with the current carrying capacity of thyristor.

A typical IGBT is shown in Fig. 4a. Those skilled in the art understand that some IGBTs are formed in striped cellular arrays of bases with sources. As shown in Fig. 4a, the IGBT 10 has an epitaxial layer 11 that includes two N⁺ source stripes regions 2a, 2b surrounded by P-typed base stripe regions 3. The portion 3a of the base 3 that lies between the source stripes is designated as the body stripe. The epitaxial layer 11 has a lightly doped N drift region 5 over a heavily doped N buffer region 7. The epitaxial layer 11 is formed on top of a heavily P doped substrate 9. On top of the device, gate insulating stripes 17, typically of silicon dioxide, cover the top of the epitaxial layer 11. Gate conductive stripes 19, typically polysilicon 19, cover the insulating stripes 17 and form a gate electrode. The gate overlies channel stripes 30a, 30b on opposite sides of the base stripe 3. Another insulating layer 21 covers the polysilicon stripes 19 and a metal contact stripe 23 contacts the source stripes 2a, 2b, N⁺ source contact regions 20 and the body stripe 3a of each cell. The above description is for a planar device with the gate on the surface. However, the IGBT may be fabricated with a trench gate. See Fig. 4b.

IGBTs may be used in ignition control circuits such as those shown in Figs. 1 and 2. Those circuits are discussed in this Background portion of the specification in order to explain the invention. The location of that discussion and the discussion itself are not admissions that the circuits are prior art. When the IGBT 10 is on, it drops a low voltage $V_{CE(sat)}$ and current flows through the primary side 12 of transformer 14. The ratio of the primary to the secondary coil 16 is about 100:1. The voltage is allowed to build to about 400 volts across the primary. When the spark plug is triggered, most of the energy is discharged in the spark. If there is any residual

energy, it is dissipated by an auxiliary clamp circuit 80. In Fig. 1 the clamp circuit 80a is a single pair or multiple pairs of Zener diodes 82, 84 with a cumulative breakdown voltage of about 400 volts. In Fig. 2 the clamp circuit 80b is a voltage divider including resistors R1, R2 and a single pair or multiple pairs Zener diodes 86.

5 After the gate signal is removed, auxiliary circuits 80 keep the IGBT 10 on in order to dissipate residual energy and prevent a localized failure.

The voltage for the auxiliary circuits 80 is set by the zener diodes to dissipate the energy over time. A problem arises if there is no spark due to, for example, a broken spark plug wire or a fouled plug. That leaves an open secondary 16 and the energy remains stored in the inductors 12, 16. With the gate turned off, the energy stored in the primary 12 cannot be transferred to the secondary 16. The primary 12 forces the voltage to rise until the zeners break down. In the self clamped inductive switching (SCIS) mode a portion of the collector current, I_{zener} , is diverted from the collector and into the gate to keep the IGBT on. Then energy stored in the primary inductor 12 will dissipate even after the gate signal is removed.

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In the SCIS mode the IGBT must absorb all the energy stored in the ignition coil during abnormal operating conditions. The most common abnormal condition is an open secondary. The silicon area of the IGBT is defined by its SCIS energy density capability. Therefore, it is imperative that the SCIS energy density (mJ/cm^2) be increased because shrinking the silicon area reduces cost and the IGBT footprint is reduced to free up module space. A 60% reduction in the footprint can be realized by offering the same SCIS capability in the DPak (TO-252) rather than a D2Pak (TO-263). Supplying the same device performance in a DPak allows the module designer to add this functionality without increasing the module size.

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In the clamping phase of the SCIS mode, a portion of the collector current is fed back to the gate after the diodes in Figs. 1 and 2 avalanche. This current develops the required gate plateau voltage $V_{GE(\text{plateau})}$ across the R_{GE} or R_2 to deliver the necessary p-n-p base electron current required to conduct the total decaying current from the energy stored in the primary coil at the clamping voltage. See Fig 3. The $V_{GE(\text{plateau})}$ continually self adjusts because it is a function of the IGBT threshold voltage (V_{th}), p-n-p current gain (α_{p-n-p}), Phase leakage current, and channel mobility (μ_{ns}). All of the above are a function of the device temperature. So $V_{GE(\text{plateau})}$ decreases with temperature because of the following factors:

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1. The V_{th} voltage has a negative temperature coefficient.
2. The α_{p-n-p} has a positive temperature coefficient, reducing the percentage of electron current to deliver the total decaying SCIS current.
3. The electron current generated from the Phase leakage current has a positive temperature coefficient. Refer to stripe cell cross-section shown in Fig 4. This reduces the amount of electron current required to drift across the channel because the leakage current can supply part of the p-n-p base current.

$V_{GE(plateau)}$ increases with temperature because the degradation in μ_{ns} with increasing temperature causes a de-biasing effect.

Factors 1, 2, and 3 outweigh factor 4. So as the device heats up and current decays $V_{GE(plateau)}$ will decrease at an accelerated rate. If $V_{GE(plateau)}$ reaches zero anywhere on the die while the temperature is still rising and an appreciable amount of current ($>1A$) is still decaying from the primary to induce localized thermal runaway, the device will fail to maintain the clamping function and may fail destructively. As such, it is desirable to find a solution for keeping $V_{GE(plateau)}$ high during SCIS clamping.

Others have tried to extend the SCIS capability by decreasing the cell pitch to more uniformly distribute the heating during SCIS by reducing the localized current density. In some designs the cell is full channel and N+ channel doping is contacted along the entire length of the stripe as showed in Fig 5. With such designs, $V_{GE(plateau)}$ during SCIS is reduced because the electron current density per unit channel width is reduced. Thus, such designs fail to improve SCIS performance. Another design to improve SCIS performance relies upon dividing the channel width into multiple segments as shown in Fig 6. The channel width is reduced by excluding the N+ channel doping. This can be accomplished by a simple lithographic bar pattern with the results shown in the bottom half of Fig 6. The N+ doping need not be continuous across the contact opening as shown in the top half of Fig 6. The segments of the channel can be connected in their centers or at their ends. See the versions showed in Figs. 7 and 8. In both figures, contact is made again along the full length of the N+ channel doping. The N+ contact areas are not required, nor must they be continuous across the contact opening. These methods increase $V_{GE(plateau)}$ and the electron current density per unit channel width. The higher electron current

per unit channel width increases the maximum peak temperature before all the IGBT p-n-p base current can be supplied by the increasing Pbase leakage current.

Summary

5 The invention improves SCIS performance by altering the structure of the source contact regions and by altering the structure of the sources. In particular, channel resistances are added to the device in order to more effectively distribute the heat across the surface of the die. The construction of the IGBT is altered so that contact to the source stripes is made only substantially through the source contact
10 regions. As such, prior art techniques that relied upon contacting the source stripes along their entire length are not used. The portion of the source stripe adjacent the body region is either excluded from doping or is suitably shielded by an insulating layer. The invention also divides source stripes along the width of the channel into a plurality of segments. These segments may be of equal length and opposite each
15 other and connected at their middles by a source contact region. In another embodiment the source stripe segments may be jogged with respect to each other so that the source contact region connects the head of one segment to the tail of another segment on the opposite side of the body stripe.

The invention provides an insulated bipolar transistor device (IGBT) that has a
20 substrate heavily doped with a first dopant of one polarity, conventionally P-type doping. Above the substrate are buffer and drift layers typically comprising N-type dopants. The buffer layer is heavily doped and adjacent the substrate. The drift layer is more lightly doped and extends to the surface of the device. The surface of the device has a number of elongated base stripe regions formed with P-type dopants.

25 Each base stripe region is bordered by the drift layer and extends along a length of the surface. The IGBT has numerous base stripes. Within each of the base stripes there are first and second source stripes. The source stripes are typically formed with N-type dopants and are located opposite each other and near the edges of their base stripe. The source stripes are essentially parallel to each other and extend in the same
30 direction as the base stripes. A region in the base stripe and between the source stripes define a body stripe of P-type dopant. Portions of the base stripe between the source stripes and the proximate bordering drift layer define channel regions for the IGBT. A gate electrode is over each channel. The gate electrodes include gate oxide stripe, a conductive gate stripe and an insulating layer over the conductive gate stripe.

A source contact layer, typically of metal, extends through vias in the insulating layer. The vias are at a number of locations aligned with the polysilicon gate and body stripe. The source contact layer fills the vias in the insulating layer and makes contact to a number of source contact regions. The source contact regions are typically heavily N-doped and are disposed in the body stripe. The source contact regions extend from the body stripe to one or both of the source stripes and are in electrical contact with the source contact layer. The insulating layer covers the portions of the source stripes that are proximate the body regions. Thus, the only contact to the source stripes is through the source contact regions.

In one embodiment, the source stripes are continuous and are periodically interconnected by source contact regions. The source contact regions and the source stripes may have the same heavy N-type doping. As an alternative, their stripes may have less of an N-type doping concentration. The invention also divides the source stripes into a plurality of elongated source segments comprising head and tail sections and elongated bodies. The source segments are spaced from each other along opposite sides of the body stripe. Portions of the body region extend between sequential head and tail sections of the segments in order to separate the sequential source stripe segments from each other. In one embodiment the source segments are the same length and are connected together at approximately the middle of their lengths by a source contact region. In another embodiment, the source stripes on either side of the body region are jogged with respect to each other. In that embodiment, the head of a source stripe on one side of the body stripe is connected across the body to the tail of another source stripe on the opposite side of the body stripe by a source contact region.

Drawings

Figs. 1 and 2 are circuit diagrams of IGBT driver circuits for automobile ignitions.

Fig. 3 is a graphic representation of operation of the IGBT before and during SCIS mode.

Figs. 4a, 4b show conventional surface gate and trench gate IGBTs.

Figs. 4c, 4d show expanded partial cross section and perspective views of a conventional surface gate IGBT.

Fig. 5 is a detailed expanded plan view of a conventional IGBT stripe cell.

Fig. 6 is a detailed expanded plan view of a conventional IGBT with source excluded sections.

Fig. 7 is a detailed expanded plan view of an IGBT stripe cell with source segments connected at their middles.

Fig. 8 is a detailed expanded plan view of an IGBT stripe cell with source segments connected head to tail.

Fig. 9 is a detailed expanded plan view of an IGBT with channel resistances.

Fig. 10 is a set of graphs comparing selected characteristics of the performance of a device made in accordance with Fig. 5 to those of a device made in accordance with Fig. 14.

Fig. 11 is another set of graphs comparing Phase temperature and voltage characteristics of devices made in accordance with Figs. 5 and 9.

Fig. 12 is a graph comparing the SCIS energy of a device made in accordance with Figs. 5 and 14.

Fig. 13 is a detailed expanded plan view of an IGBT stripe cell with channel resistances and source segments connected at their middles.

Fig. 14 is a detailed expanded plan view of an IGBT stripe cell with channel resistances and source segments connected head to tail.

Fig. 15 is a partial expanded plan view of the invention in a trench gated IGBT with channel resistors along the width of the gate.

Fig. 16 is a partial expanded plan view of the invention in a trench gated IGBT with segmented sources contacted at their middles.

Fig. 17 is a partial expanded plan view of the invention in a trench gated IGBT with segmented sources contacted at their respective heads and tails.

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Detailed Description

Details of the structure of typical prior art devices are shown in Figs. 4c and 4d. Those figures show two source stripes 2a, 2b within base strip 3. The gate electrodes 19a, 19b overly portions of the gate stripes to 2a, 2b and outer portions of the base stripe 3. The electrodes 19a, 19b induce channels 30a, 30b between the outer edges of the source stripes 2a, 2b and the drift layer 5. Dielectric stripes 21a, 21b enclose the upper portions of the gates 19a, 19b and have vias 40 for source contact metal. In a conventional IGBT the source contact metal 40 makes electrical and mechanical contact with source contact diffusion regions 20a, 20b,...20n as well as inside portions of the source strips 2a, 2b. Note that the inside portions designated 41a, 41b are contacted by the source metal 23.

Fig. 5 is a detailed plan of a portion of a stripe cell in the structure as illustrated in Figs. 4a, 4c and 4d. The central portion shows two channel stripes 2a, 2b in base stripe 3 that are separated by portion 3a of the base stripe. N⁺ contact regions 20a, 20b, 20c are shown. Likewise, the source metal contacted regions 41a, 41b of the source stripes 2a, 2b are also shown. The source metal makes contact with the exposed portions of the N⁺ contact regions 20 and the portions 41a, 41b of the stripes 2a, 2b. Thus, the entire width of the channel is contacted by the source metal. That structure does not improve SCIS performance.

Fig. 6 shows one attempt to improve performance of the IGBT by dividing the source stripes into numerous source contact regions 20. Some of these regions extend across most of the base 3 to provide channel regions. See for example source contact regions 20a – 20d. Other source contact regions such as 20e and 20f are spaced on opposite sides of the base stripe. It is not necessary that the source contact regions 20 be continuous across the base stripe 3. The structure shown in Fig. 6 is formed by providing a suitable mask that will exclude N⁺ source regions from undesired areas and leave only the Pbase 3 in those areas.

Figs. 7 and 8 show further examples of speculative structures that can be made with prior art techniques. No admission is made in this application that Figs. 7 and 8

are, per se, prior art. One could divide the gate stripe 2 into a plurality of segments such as 2a.1 that is opposite segment 2b.1 and segment 2a.2 that is opposite segment 2b.2...2a.n opposite 2b.n. Each of the pairs of segments 2a.n., 2b.n are connected near the middle of their length by a heavily doped N+ contact 20. As such, N+ contact 20b connects source segments 2a.2 and 2b.2. The regions 30a, 30b,...30n between the heads (H) and the tails (T) of the sequential source segments are P-doped as is the Pbase. A jogged or z-type structure is shown in Fig. 8. There, the head of a striped segment on one side is connected to the tail of the next sequential source stripe on the opposite side of the base 3. So, the head of source stripe segment 2a.1 is connected via N+ contact region 20b to the tail of source stripe segment 2b.2.

The invention overcomes the problems of the prior art by isolating the source stripes from the source metal contact to increase the resistance of the channel along the width of the channel. In the embodiment shown in Fig. 9, these results are achieved by narrowing the source stripes 2a, 2b or extending the dielectric 21a, 21b so that the source stripes are entirely disposed beneath the dielectric layers 21a, 21b and are not contacted by the source metal 23. As such, the only contact to the source stripes 2a, 2b is through the periodic source contact regions 20. The stripes 2a, 2b remain continuous along the length of the base stripe 3. The source stripes on opposite sides of base stripe 3 are periodically connected together by N+ contact regions 20. That structure provides channel resistance along the width of the source stripes 2a, 2b. The resistance between two sequential contact areas 20a, 20b is greatest in the middle. As such, the channel resistors concentrate current near the source contact regions 20. The wider the spacing between the contacts 20, the larger the resistive drop to the midpoint between two N+ contacts 20 and the higher the N+ source contact resistance due to reduced contact area. The N+ contacts can be continuous across the contact opening or extend partially across as shown in the top portion of Fig. 6. The channel resistors function to locally offset decreases in V_{GE} (plateau) by constricting the flow of the electron current to smaller areas as the temperature increases due to the positive temperature coefficient of the resistor. While the larger spacings (50um or greater) between N+ contacts further offset the decrease in V_{GE} (plateau) due to the increased contact resistance. When temperature rises in a certain area of the die due to SCIS induced self-heating, the voltage drop down the length of the local resistor and at the N+ contacts increases. The highest voltage drop is furthest from the N+ contact. Thus, a gradual de-biasing of the gate occurs along

the channel resistor to the N+ contact. At room temperature, the de-biasing effect is small. An electron current flows through the channel almost uniformly down the length of the resistor. However, as the temperature increases and the current continues to decay, the conduction of the electron current through the channel starts to constrict along the entire channel resistor length to smaller areas directly across from the N+ contacts 20. This effectively reduces the channel width of the IGBT. The reduction in effective channel width of the IGBT forces the gate to maintain a higher bias to pass the total current. The effect of this structure is demonstrated in Fig. 10.

There the V_{GE} (plateau) of the full channel design (Fig. 5) decays linearly. However, the V_{GE} (plateau) is higher for the channel resistor design and has a non-linear decay because the electron current is constricted as the temperature increases. The constriction of electron current into these smaller areas increases the maximum peak temperature before all the IGBT p-n-p base current can be supplied by the increasing Phase leakage current. When this occurs, the IGBT gate control is lost, thermal runaway occurs, and the clamping function fails. This is demonstrated by the simulated wave forms in Fig. 11. Although the increase in channel resistance due to the temperature effect was not modeled, the simulations show that the device must reach 30°C to 40°C higher peak Phase temperature for the clamping function to fail on the device with the channel resistance invention compared to the full channel device of Fig. 5. The temperature difference would be higher with the channel resistance temperature affect included. The measured comparison in SCIS energy density improvement as a function of starting junction temperature at the initiation of the SCIS mode is shown in Fig. 12. There it can be seen that the SCIS energy density is uniformly higher for the channel resistor as compared to the full channel for all temperatures.

The invention can also be applied to segmented source structures. Examples of the invention of such structures are shown in Figs. 13 and 14. Fig. 13 has the source segments 2a and 2b disposed on opposite sides of the base stripe 3 and separated by the body 3a. Note: that the contact opening is sized with the narrower source stripes 2a, 2b so that only the source contact regions 20 are available for contact. The heads and tails of sequential sources are separated by the Phase region 3.

Fig. 14 adapts a z-shaped structure to the invention. There the source stripes 2a are jogged with respect to the source stripes 2b. As such, the head of one source stripe 2a.1 terminates at about a location where an opposite, jogged source stripe tail

of 2b.2 begins. The source stripes are connected by N+ contacts 20a.1, 20a.2. As mentioned above, the contact may be continuous or may be interrupted. Either structure is suitable for the invention.

Having thus described the invention and several embodiments thereof, those skilled in the art will appreciate that further modifications, additions and omissions of elements may be made to the invention without departing from the spirit and structure as set forth in the claims. In particular, the invention can be adapted to trench gated IGBTs such as the samples shown in Fig. 4b. Turning to Fig. 15, the invention is showed in a trench gated IGBT. The gate polysilicon 19 is in the middle. Source stripes 2a, 2b and base stripes 300a, 300b are separated by the gate oxide 17 that cover the walls of the trench. The insulating layer 21 extends over the gate, over the source stripes 2a, 2b and over a portion of the base stripes 300a, 300b. Source contact regions 20nl and 20nr contact the source stripes 2a, 2b on opposite sides of the gate trench. Channel resistances CR are formed in the portions of the source stripes between the contact regions. This embodiment of the invention is similar to the planar gate embodiment shown in Fig. 9. Figs. 16 and 17 show other trench gate embodiments that are similar respectively to the planar embodiments showed in Figs. 13 and 14, respectively. In Fig. 16 selected portions of the source stripe are excluded to form source segments of equal length. The segments on opposite sides of the trench are contacted. In Fig. 17 source segments are jogged with respect to each other. Segments on opposite sides of the trench have source contacts at opposite heads and tails.

Those skilled in the art will understand that the invention may be embodied in other configurations. For example, the lengths of the channel resistors may be different depending upon their location. In general, shorter lengths closer to the center of the die are preferred. In addition opposing segments of the embodiment shown in Figs. 13, 14 and 15, 16 do not have to be the same length. Similar results can be achieved by masking and doping the source stripes and source segments to alter the resistance of the channel resistors. Those skilled in the art also understand that the base stripes may be connected together at their ends to form a common base for the device.